UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,759	08/04/2000	Richard J. Selvaggi	ATI-000118BN	2358

25310 7590 07/01/2004

VOLPE AND KOENIG, P.C.
DEPT. ATI
UNITED PLAZA, SUITE 1600
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103

EXAMINER	
AMINI, JAVID A	

ART UNIT	PAPER NUMBER
2672	11

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,759	SELVAGGI ET AL.	
	Examiner	Art Unit	
	Javid A Amini	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5-6, 7-9, 11-12, 13-15, and 17-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-6, 7-9, 11-12, 13-15, and 17-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Ashburn U.S. patent 5,651,106, dated July 22, 1997, and further in view of Hsieh et al. (hereinafter referred as a Hsieh).

1. Claim 1.

A method for processing video image data including a plurality of different image data types, the method comprising the steps of: providing a set of tasks to be performed on each different image data type, each task including one or more basic state operation, each basic state operation being a single arithmetic operation; Ashburn on col. 8, lines 63-67, and also see Fig. 2, discloses that In an alternative embodiment, both the left and right stacks contain identical hardware, including dividers. In this configuration, functionality may be partitioned such that each stack performs the same operations on different primitives. Applicant does not explicitly specify the definition of claim language of a single arithmetic operation and basic state operations; therefore, Ashburn in Fig. 6 illustrates a single arithmetic operation for edge 1.

Ashburn in Fig. 11 shows the basic state operations under calculate column. Dividing the image data into a plurality of groups based on the image data type, sorting the basic state operations from all of the image data groups based on the arithmetic operation type; Ashburn does not explicitly specify sorting the basic state operation from the image data. But Ashburn on col. 9, lines 43-55 teaches the graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of sorting in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. However Hsieh on page 1 paragraph 0005 discloses the single instructions multiple data (SIMD) processes multiple data elements simultaneously. Now Hsieh in figs. 3 the data elements A, B, C, and D, of a first operand 310 are multiplied with the respective E, F, G, and H packed data elements (i.e. equivalent to applicant's claim language "data group based on the operation") of a second operand 312 to generate a result 316. Assigning each sorted basic state operation to one of a plurality of commonly used arithmetic units based on the corresponding arithmetic operation type, wherein all basic state operations of the same arithmetic operation type are assigned to the same arithmetic unit; Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188 (considered to be basic state operations) respectively perform multiplies and divides. Hsieh in fig. 2 illustrates it clearly the claim language, as assigning a parallel operation denoted by the operator "o", involves two operands, a first operand 210 and a second operand

220, to produce a result 230. The term "operand" is interchangeably used herein to refer to the data on which an instruction operates or the storage area (e.g., register, memory location, etc.) in which that data can be found. Each of the operands 210 and 220 is a packed data item, comprising four separate data elements, each data element is 32-bit wide for a total operand size of 128-bit. In one embodiment, each data element in a packed data item is a floating-point number. In another embodiment, each data element in a packed data item is an integer number. One skilled in the art that any number of data elements in each operand and any data element size for each data element can be utilized will appreciate it. One will further appreciate it skilled in the art that the data element sizes in each operand may be different. Performing each basic state operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided set of tasks; and combining the transformed image data of each group. Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive. Hsieh in figs. 2, 3, 5, 7A-B and 8-9 illustrates combining the transformed data of each group or packed. Note: Hsieh in fig. 2 illustrates an equivalent of assigning operation to each packed data, (for example: A0 and B0 packed data are assigned to the operation, denoted by the operator "o"). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate

the teaching of Hsieh into Ashburn in order the operation performs in less time. By modifying the SIMD into fig. 3 of Ashburn to eliminate the fetching processes.

2. Claim 2.

"The method of claim 1 wherein the plurality of image data groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". See rejection of claim 1.

3. Claim 3.

"The method of claim 1 wherein the plurality of said commonly used arithmetic units includes an addition unit and a multiplication unit". See rejection of claim 1.

4. Claim 5.

"The method of claim 1 further comprising the step of providing a queue for each of the plurality of commonly used arithmetic units wherein each assigned arithmetic operation is sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is obvious because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

5. Claim 6.

"The method of claim 5, wherein the basic state operations of each task can be performed by different arithmetic units, the basic state operations to be performed in a predetermined sequence, the method further comprising the step of preventing the basic state units from performing the arithmetic operations of a task out of sequence". This step is obvious because if the design of a task is correct, the arithmetic operations will follow the sequence, otherwise the task operates out of sequence.

6. Claim 7.

An apparatus for processing video image data including a plurality of different image data types, the apparatus comprising: means for providing a set of tasks to be performed on each different image data type, each task including one or more basic state operation, each basic state operation being a single arithmetic operation; Ashburn on col. 8, lines 63-67, and also see Fig. 2, discloses that In an alternative embodiment, both the left and right stacks contain identical hardware, including dividers. In this configuration, functionality may be partitioned such that each stack performs the same operations on different primitives. Applicant does not explicitly specify the definition of claim language of a single arithmetic operation and basic state operations; therefore, Ashburn in Fig. 6 illustrates a single arithmetic operation for edge 1. Ashburn in Fig. 11 shows the basic state operations under calculate column. Dividing the image data into a plurality of groups based on the image data type, sorting the basic state operations from all of the image data groups based on the arithmetic operation type; Ashburn does not explicitly specify sorting the basic state operation from the image data. But Ashburn on col. 9, lines 43-55 teaches the graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle

may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of sorting in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. However Hsieh on page 1 paragraph 0005 discloses the single instructions multiple data (SIMD) processes multiple data elements simultaneously. Now Hsieh in figs. 3 the data elements A, B, C, and D, of a first operand 310 are multiplied with the respective E, F, G, and H packed data elements (i.e. equivalent to applicant's claim language "data group based on the operation") of a second operand 312 to generate a result 316. **Means for dividing the image data into a plurality of groups based on the image data type; means for sorting the basic state operations from all of the image data groups based on the arithmetic operation type**; Ashburn on col. 9, lines 43-55 discloses that the graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of filtering in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. **Means for assigning each sorted basic state operation to one of a plurality of commonly used arithmetic units based on the corresponding arithmetic operation type, wherein all basic state operations of the same arithmetic operation type are assigned to the same arithmetic unit**; Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188

(considered to be basic state operations) respectively perform multiplies and divides. **Means for performing each basic state operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided set of tasks; and mean for combining the transformed image data of each group**". Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188 (considered to be basic state operations) respectively perform multiplies and divides. Hsieh in fig. 2 illustrates it clearly the claim language, as assigning a parallel operation denoted by the operator "o", involves two operands, a first operand 210 and a second operand 220, to produce a result 230. The term "operand" is interchangeably used herein to refer to the data on which an instruction operates or the storage area (e.g., register, memory location, etc.) in which that data can be found. Each of the operands 210 and 220 is a packed data item, comprising four separate data elements, each data element is 32-bit wide for a total operand size of 128-bit. In one embodiment, each data element in a packed data item is a floating-point number. In another embodiment, each data element in a packed data item is an integer number. One skilled in the art that any number of data elements in each operand and any data element size for each data element can be utilized will appreciate it. One will further appreciate it skilled in the art that the data element sizes in each operand may be different. Performing each basic state operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided set of tasks; and combining the transformed image data of each group. Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant

texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive. Hsieh in figs. 2, 3, 5, 7A-B and 8-9 illustrates combining the transformed data of each group or packed. Note: Hsieh in fig. 2 illustrates an equivalent of assigning operation to each packed data, (for example: A0 and B0 packed data are assigned to the operation, denoted by the operator "o"). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Hsieh into Ashburn in order the operation performs in less time. By modifying the SIMD into fig. 3 of Ashburn to eliminate the fetching processes.

7. Claim 8.

"The apparatus of claim 7 wherein the plurality of image data groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". See rejection of claim 7.

8. Claim 9.

"The apparatus of claim 7 wherein the plurality of said commonly a used arithmetic unit includes an addition unit and a multiplication unit". See rejection of claim 7.

9. Claim 11.

"The apparatus of claim 7 further comprising a queue for each of said commonly used arithmetic units and wherein each basic state operation is sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data

representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is obvious because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

10. Claim 12.

"The apparatus of claim 11, wherein the basic state operations of a task are to be performed in a predetermined sequence, the apparatus further comprising means for preventing the arithmetic units from performing the basic state operation of a task out of sequence". This step is obvious because if the design of a task is correct the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

11. Claim 13.

"**An apparatus for performing video processing, the video processing including performing a set of tasks on vertex parameters, the apparatus comprising: a scheduler having an input configured to receive the set of tasks, said scheduler arranging the vertex parameters to be processed into a plurality of groups based on in part characteristics of the vertex parameters;** Ashburn on col. 8, lines 63-67, and also see Fig. 2, discloses that In an alternative embodiment, both the left and right stacks contain identical hardware, including dividers. In this configuration, functionality may be partitioned such that each stack performs the same operations on different primitives. Applicant does not explicitly specify the definition of claim language of a single arithmetic operation and basic state operations; therefore, Ashburn in Fig. 6 illustrates a single arithmetic operation for edge 1. Ashburn in Fig. 11 shows the basic

state operations under calculate column. **A sequencer for each group, said sequencer: selecting the tasks required to process that group's parameters**; Ashburn on col. 6, lines 36-41 discloses that unlike conventional texture mapping systems that download the entire series (sequence) of MIP maps for any primitive being rendered, the present invention downloads only the portion of the series of MIP maps actually needed to currently render the primitive or the currently rendered portion thereof. **Determining a set of basic state operations required to accomplish that group's tasks, wherein each basic state operation is a single arithmetic operation; sorting the basic state operations from all of the image data groups based on the arithmetic operation type;** Ashburn on col. 9, lines 43-55 discloses that the graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of filtering in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. **Assigning each sorted basic state operation to be performed to one of a plurality of commonly used arithmetic units based on the corresponding arithmetic operation type, wherein all basic state operations of the same arithmetic operation type are assigned to the same arithmetic unit;** Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188 (considered to be basic state operations) respectively perform multiplies and divides. Ashburn does not explicitly specify sorting the basic state operation from the image data. But Ashburn on col. 9, lines 43-55 teaches the

graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of sorting in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. However Hsieh on page 1 paragraph 0005 discloses the single instructions multiple data (SIMD) processes multiple data elements simultaneously. Now Hsieh in figs. 3 the data elements A, B, C, and D, of a first operand 310 are multiplied with the respective E, F, G, and H packed data elements (i.e. equivalent to applicant's claim language "data group based on the operation") of a second operand 312 to generate a result 316. **And sending each of the basic state operations of each of that group's tasks to the arithmetic unit associated with that basic state operation; and each of said commonly used arithmetic units, having an input configured to receive the sent basic state operations and vertex parameters associated with the sent operations, each arithmetic unit performing the sent basic state operations on the sent vertex parameters**; Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R, G, B color control signals for each pixel are respectively provided over R, G, B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive. Hsieh in fig. 2 illustrates it clearly the claim language, as assigning a parallel operation denoted by the operator "o", involves two operands, a first operand 210 and a second operand 220, to produce a result 230. The term

"operand" is interchangeably used herein to refer to the data on which an instruction operates or the storage area (e.g., register, memory location, etc.) in which that data can be found. Each of the operands 210 and 220 is a packed data item, comprising four separate data elements, each data element is 32-bit wide for a total operand size of 128-bit. Each data element in a packed data item is a floating-point number. Each data element in a packed data item is an integer number. One skilled in the art that any number of data elements in each operand and any data element size for each data element can be utilized will appreciate it. One will further appreciate it skilled in the art that the data element sizes in each operand may be different. Performing each basic state operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided set of tasks; and combining the transformed image data of each group. Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive. Hsieh in figs. 2, 3, 5, 7A-B and 8-9 illustrates combining the transformed data of each group or packed. Note: Hsieh in fig. 2 illustrates an equivalent of assigning operation to each packed data, (for example: A0 and B0 packed data are assigned to the operation, denoted by the operator "o"). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Hsieh into Ashburn in order the operation performs in less time. By modifying the SIMD into fig. 3 of Ashburn to eliminate the fetching processes.

12. Claim 14.

"The apparatus of claim 13 wherein the plurality of groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". Ashburn illustrates in Fig. 1A that the distributor chip 30 receives the X,Y,Z coordinate and color primitive data over bus 16 from the host computer, and distributes 3-D primitive data evenly among the 3-D geometry accelerator chips 32A, 32B and 32C. The texture mapping data transfers over bus 94. In this manner, the system bandwidth is increased because three groups of primitives are operated upon simultaneously.

13. Claim 15.

"The apparatus of claim 13 wherein said plurality of said commonly a used arithmetic unit includes an addition unit and a multiplication unit". See rejection of claim 13.

14. Claim 17.

"The apparatus of claim 13 further comprising a queue for each of said commonly used arithmetic units and wherein the sent basic state operations are sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is obvious because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

15. Claim 18.

"The apparatus of claim 17 wherein the basic state operations of a task are to be performed in a predetermined sequence and said sequencer prevents said arithmetic units from performing the basic state operations of a task out of sequence". This step is obvious because if the design of a task is correct the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Javid A Amini
Examiner
Art Unit 2672

JEFFERY BRIER
PRIMARY EXAMINER

Javid Amini